REMARKS

Claim 7 is amended herein. Claims 1-8 and 10-23 remain pending in the application.

35 USC 112 First Paragraph Rejection of Claims 7 and 8

The Office Action rejected claims 7 and 8 under 35 USC 112 first paragraph.

In particular, it should be noted that while the language "variable" has been removed from claim 7, claim 7 none the less reads on a variable clock signal.

Claim 7 have been reviewed and are amended where appropriate. It is respectfully submitted that the claims are now in full conformance with 35 USC 112. It is respectfully requested that the rejection be withdrawn.

Claims 17-19 and 22 over Persaud

In the Office Action, claims 17-19 and 22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated be Persaud et al., UK Patent Application No. GB2074762 ("Persaud"). Applicants respectfully traverse the rejection.

Claims 17-19 and 22 recite, *inter alia*, accessing a portion of an external non-dedicated shared memory from a second agent based on a representation of a memory access clock signal received **from a first agent**.

Persaud appears to teach a system and method for accessing a common memory by a plurality of processors (Persaud, Abstract). A master processor can access its own memory or any of the slave memories (Persaid, Abstract). The master processor generates synchronizing signals which are applied over a backplane to each of the slave processors (Persaud, page 2, lines 45-47). Numerous clocks start to cycle during a POWER ON RESET signal during a reset of a clock generator (Persaud, page 5, lines 48-50). Clock synchronization between the master processor and slave processors is accomplished by sending a REFRESH REQ from the master card to the slave cards (Persaud, page 5, line 60 – page 6, line 16).

Persaud utilizes processors that are driven by separate dedicated clocks that are normally sychronized, but can become de-synchronized (Persaud, page 2, lines 45-47; page 6, lines 10-11). A synchronization signal from the master processor is used to synchronize the various clocks within the slaves. A master processor is synchronized with the slave processor and accesses a slave processor's dedicated memory based on the synchronization of all clocks within the system. Persaud's memory clock signals are received from local clocks, albeit synchronized, **NOT** from a second agent based on a representation of a memory access clock signal received from a first agent, as claimed by claims 17-19 and 22.

A benefit of having a second agent access a shared memory with a clock signal received **from a first agent** is, e.g., synchronization through simplicity. Applicants' system requires only a single memory access clock, with all agents sharing the signal. A single memory access clock signal synchronizing all agents' access to a shared memory possibly eliminates wasted clock cycles during a transfer of access from a first agent to a second agent. In contrast, Persaud requires the use of a dedicated clock generator for each agent. Having multiple clock generators creates the problem of synchronization (as discussed by Persaud, page 3, lines 1-22).

Accordingly, for at least all the above reasons, claims 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-6 and 10-12 over Persaud and Luan

In the Office Action, claims 1-6 and 10-12 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Luan et al., U.S. Patent No. 5,911,149 ("Luan"). Applicants respectfully traverse the rejection.

Claims 1-6 and 10-12 recite, *inter alia*, a second agent receiving a memory access clock signal **from a first agent**.

As discussed above, Persaud teaches that a master processor sends synchronization signals to the other processors within the system to

synchronize their clocks. Each processor within the system has a dedicated clock source for access to slave processor's dedicated memory.

The Office Action relies on Luan to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention. The Applicants respectfully disagree.

Luan appears to teach a computer system having a processor and at least one peripheral having a programmable shared memory system (Abstract). A first portion of the memory is used by the processor which allocates a second portion of memory for share use by the processor and any peripherals in the system (Abstract).

Luan fails to teach how access to the shared portion of the memory system is synchronized between the processor and pheripherals. Luan makes no mention of how clock signals are routed throughout the system.

Neither Persuad nor Luan disclose, teach, or suggest a second agent receiving a memory access clock signal **from a first agent**, as claimed by claims 1-8, 10-13, 15, 16, 20, 21 and 23.

Accordingly, for at least all the above reasons, claims 1-8, 10-13, 15, 16, 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 13-16 over Persaud in view of Muthal

In the Office Action, claims 13-16 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Muthal, U.S. Patent No. 5,815,167 ("Hughes"). The Applicants respectfully traverse the rejection.

Claims 14, 15, 17-19 and 22 recite, *inter alia*, a second agent receiving a memory access clock signal **from a first agent**.

As discussed above, Persaud fails to teach a second agent receiving a memory access clock signal **from a first agent**, as claimed by claims 13-16.

Muthal appears to teach a computer system comprising a graphics controller, a memory controller and shared memory (Abstract). The shared memory is accessible by both the memory controller and graphics controller

(Muthal, Abstract). Concurrent access to portions of the shared memory is given to the graphics controller and the memory controller (Muthal, Abstract).

Muthal fails to teach how access to the shared portion of the memory system is synchronized between the processor and the graphics controller. Muthal makes no mention of how clock signals are routed throughout the system.

Neither Persuad nor Muthal disclose, teach, or suggest a second agent receiving a memory access clock signal **from a first agent**, as claimed by claims 13-16.

Accordingly, for at least all the above reasons, claims 13-16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 20, 21 and 23 over Wu and Persaud

In the Office Action, claims 20 and 21 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu et al., Patent No. 5,659,715 ("Wu") in view of Persaud, with claim 23 rejected as obvious over Wu. Applicants respectfully traverse the rejection.

Claims 20, 21 and 23 recite, *inter alia*, a second agent receiving a memory access clock signal from a first agent.

As discussed above, Persaud fails to teach a second agent receiving a memory access clock signal **from a first agent**, as claimed by claims 20, 21 and 23.

Wu appears to teach a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (WU, Fig. 3) Thus, the CPU, the graphics controller and the common memory are

synchronized to pass data and address information therebetween with a common clock signal.

Wu teaches utilizing a common clock signal for components accessing a common memory. A common clock signal is NOT a second agent receiving a memory access clock signal from a first agent, as claimed by claims 20, 21 and 23.

Neither Persuad nor Wu disclose, teach, or suggest a second agent receiving a memory access clock signal from a first agent, as claimed by claims 20, 21 and 23.

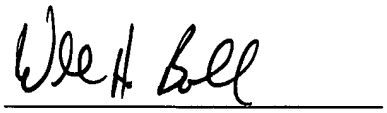
Accordingly, for at least all the above reasons, claims 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8 and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



William H. Bollman
Reg. No. 36,457

Manelli Denison & Selter PLLC
2000 M Street, NW
Suite 700
Washington, DC 20036-3307
TEL. (202) 261-1020
FAX. (202) 887-0336

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